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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

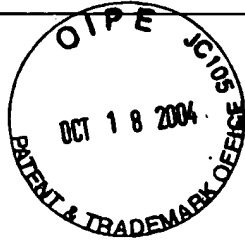
Applicant(s): Jeong

Serial No.: 10/829,593

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Title: APPARATUS AND METHOD FOR
POLISHING SEMICONDUCTOR
WAFERS USING ONE OR MORE
POLISHING SURFACES

Attorney Docket No.: INK-002



Group Art Unit: 3723

Examiner: Unknown

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97(c) together with either a:
- ☐ Statement under 37 CFR 1.97(e), or
 - ☐ a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97(d) together with a:
- ☐ Statement under 37 CFR 1.97(e), and
 - ☐ a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

☒ Applicant(s) submit herewith Form PTO 1449-Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

The relevance of the attached references is that this is the closest art of which Applicant is aware. Applicant submits that the above references taken alone or in combination neither anticipate nor render obvious the present invention. Consideration of the foregoing in relation to this application is respectfully requested.

It is requested that the information disclosed herein be made of record in this application.

I hereby certify that this is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR § 1.10 on the date indicated below and is addressed to:

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Date of Deposit: October 18, 2004

Respectfully submitted,

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CONCISE EXPLANATION OF 2003-0067391 REFERENCE

The first figure shows a CMP apparatus that includes in part two polishing modules PM1 and PM2, three loading devices 21, 22 and 23, a wafer transfer device 16 and a cleaning unit 40.

In a serial mode, the wafer transfer device 16 transfers a wafer to be polished to the loading device 21. The loading device 21 transfers the wafer to the polishing module PM1, where the wafer is polished. The loading device 22 transfers the wafer from the polishing module PM1 to the polishing module PM2, where the wafer is further polished. The loading device 23 transfers the wafer from the polishing module PM2 to the wafer transfer device 16. The wafer transfer device 16 transfers the wafer to the cleaning unit 40.

In a first parallel mode, the wafer transfer device 16 transfers wafers to be polished to the loading devices 21 and 23, respectively. The loading device 21 transfers the wafer to the polishing module PM1, where the wafer is polished. The loading device 23 transfers the wafer to the polishing module PM2, where the wafer is polished. After the wafers are polished, the loading device 22 transfers the wafers from the polishing modules PM1 and PM2 to the wafer transfer device 16.

In a second parallel mode, the wafer transfer device 16 transfers wafers to be polished to the loading device 22 which transfers the wafers to the polishing modules PM1 and PM2, respectively. The wafers polished in the polishing modules PM1 and PM2 are unloaded to the loading devices 21 and 23, respectively, and then transferred to the wafer transfer device 16.

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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